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THE USE OF WATCHDOG TIMER FOR RESTORATION OF MICROPROCESSOR SYSTEMS WITH ENHANCED FAULT TOLERANCE TO INFLUENCE OF ELECTROSTATIC DISCHARGES

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Анотація. *Мікропроцесорні системи, призначені для тривалої безперервної роботи в автономному режимі, повинні забезпечувати мінімальний час простою протягом їх терміну служби. Вплив електростатичних розрядів на мікропроцесорну систему може викликати її «пошкодження». Пошкодження системи є причиною появи «збою» – самоусуваються відмови або відмови, які усуваються незначним втручанням оператора. Ця відмова може призводити до «зависання» мікропроцесорної системи, що збільшує час простою системи, знижує ефективність її використання. За результатами дослідження поведінки систем при відмовах як в лабораторних умовах, так і безпосередньо в умовах об'єктів, розроблені принципова електрична схема і алгоритм роботи зовнішнього по відношенню до мікропроцесора сторожового таймера, який дозволяє відновити працездатність мікропроцесора автономних систем після впливу електростатичних розрядів, що не перевищують поріг руйнування, шляхом перезапуску його за живленням в автоматичному режимі. Представлена і впроваджена в експлуатацію апаратно-програмна реалізація розробленого методу підвищення відмовостійкості до впливу електростатичних розрядів. Ефективність цього технічного рішення підтверджується результатами експлуатації протягом декількох років декількох сотень мікропроцесорних систем на різних об'єктах України військового, промислового, житлового та комунального призначення. Вирішення цієї проблеми було здійснено автором даної статті на рівні абсолютної світової новизни, що підтверджено патентом.*
Ключові слова: *мікроконтролер, електростатичний розряд, відмовостійкість, пошкодження, відмова, вид відмови, стан зависання мікроконтролера, працездатність, перезапуск мікроконтролера.*

Abstract. *Microprocessor systems, which are designed for long-term continuous operation in a standalone mode, must provide a minimum downtime during their exploitation. The impact of electrostatic discharges on a microprocessor system can cause its damage. Damage to the system is the cause of its malfunction that can be either a self-resolving failure or a failure which is eliminated by minor operator intervention. This failure can lead to a hang of the microprocessor system which increases the system downtime and reduces the efficiency of its usage. According to the results of the study of the behavior of systems under failure both in laboratory conditions and directly at enterprises, a basic electrical circuit and an algorithm for the operation of an external watchdog timer relative to the microprocessor have been developed which allows to restore the microprocessor of autonomous systems after its exposure to electrostatic discharges that do not exceed the destruction threshold by restarting it by power in the automatic mode. The hardware and software implementation of the developed method for increasing the fault tolerance to the effects of electrostatic discharges is presented and put into operation. Efficiency of this technical solution is confirmed by the results of the exploitation during a few years of several hundred microprocessor systems at various Ukrainian enterprises for military, industrial, residential and municipal purposes. The solution of this problem had been performed by the author of this article at the level of absolute world novelty what is confirmed by a patent.*
Keywords: *microcontroller, electrostatic discharge, fault tolerance, damage, failure, types of failure, hang, work capacity, microcontroller restart.*

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1. Introduction

Among the requirements for the electronic base of microprocessor systems, which are designed for long-term continuous operation in a standalone mode, one of the most important is the requirement to automatically restore work capacity of specialized microprocessors – microcontrollers (MC) – in the event of failures associated with the effects of electrostatic discharges (ESD) during the exploitation of these systems.

As a rule, the impact of electrostatics leads to the accumulation of damage in microcontrollers and their framing. These damages may cause non-fatal failures of the object. Under long-lasting impact such damages become fatal failures. This complicates the exploitation of autonomously operating system devices [1].

The paper provides a review of scientific and technical works on the mechanisms of failure, defects and damages in microprocessor systems and makes conclusions which are the basis for solving this problem [2]. Thus, the works of Piskun H.A. and Alekseev V.F. note the increased sensitivity of microcontrollers to ESD, in connection with which the task of analyzing the mechanisms of failures, defects and damages in microprocessor systems is extremely important [3]. In the works of Horlov M.I. and Strohonov A.V. relative sensitivity of different types of integrated circuits (IC) to ESD is studied [4]. The issues of classifying basic mechanisms of damage of modern types of IC to ESD exposure, systematization of ESD by the type of exposure and mechanism of influence on equipment, classification of discharge gradations by the degree of damage, as well as identification of areas of damage are considered in the works by Bryleva O.A., Piskun H.A. and Alekseev V.F. [5]. The questions of electrostatic protection of input-output elements of integrated circuits made on submicron high-voltage CMOS technology are considered in the works of Karpovych M.S. and Lys V.D. [6]. In the works of Abrameshyn A.E. the use of weakly conducting dielectric composite radio materials in printed circuit boards (PCB) is substantiated. It provides redistribution of the accumulated charge, alignment of electrostatic potentials and prevention of ESD on PCBs [7]. In the works of Piskun H.A. and Alekseev V.F. [8] there is presented a promising research aimed at solving this problem. The mentioned research was conducted in the field of determining critical (threshold) values of voltages affected by ESD.

Below there are discussed some known hardware and software solutions which do not solve the problem of automatic restoration of work capacity of a microprocessor device damaged by ESD. The author of the article has developed a method for restoring work capacity of the systems in case of such failure [2].

The aim of this paper is to increase fault tolerance of microprocessor devices to the effects of ESD based on the development of a hardware-software solution according to the proposed method which provides automatic restart of the microcontroller after a hang in the case of exposure to ESD. The solution of this problem had been performed by the author of this article at the level of absolute world novelty what is confirmed by a patent [9].

2. Problem statement

A method for removing a product containing a microprocessor board from a hang was proposed in [2]. It has been found that the cause of the failure is clearly the effect of ESD. In addition, the mechanism of damage to integrated circuits under the influence of ESD was studied in [2]. These circumstances explain the reason for the recovery of microprocessor boards after turning off the power of the boards in the manual mode. In the author's opinion, the reason for it is the removal of the electric charge which can accumulate in the area of damage to the structure of the integrated circuit what leads to the integrated circuit inoperability. Performance is restored after removing the electric charge, although damage to the integrated circuit is not eliminated. Therefore, the

objective of this work is to develop a hardware-software solution for the automatic output of a microprocessor from the inoperative state. This hardware- software solution should be as simple and reliable as possible, contain a minimum number of electronic components and not complicate the principles of product construction. The effectiveness of the solution should be confirmed by positive results of its operation over a period of time that is comparable to the useful life of the product on a significant number of products. The size of this sample of products should be large and representative.

3. Literature review

In microprocessor systems, a system reset is performed for each of three events [10]: when the power is turned on by the signal from the corresponding button, when a gap is detected, or when the control signal hangs (stops changing). As a device that generates Reset System pulses (RST), a Watchdog Timer (WDT) (either a hardware-software watchdog timer built into the MC or an external watchdog timer that will perform a system reset (restart, reboot) at the RST MC input) is used. So, the hardware-software WDT built into the MC of the Atmel MCS-51 and AVR families from Atmel generates a MC reset at the software and hardware level if the program performs uncontrolled actions, for example, it hangs [11]. The disadvantage of this technical solution is the embeddedness of the WDT into the MC. When the program hangs, it often leads to the WDT inoperability.

A known method for recovering an inoperable MC from the hang is its external restart at the RST input, in case when the parameters of the MC operability signal deviate from the set ones. The signal is controlled by an external WDT. Among external WDTs that are manufactured as integrated circuits and implemented into the MC there are: Maxim MAX6751, Texas Instruments TPS3126, Analog Devices ADM699, ADM6316, ADM8323, ADM8324. In general, operation of the MC equipment is not controlled by the software. Therefore the failure of the MC cannot affect the operation of the external WDT.

The integrated circuit ADM8324 [12] contains a WDT, to which a detector of actuation of the WDT chip is connected. The detector output is connected to the MC restart pulse generator. The output of the generator through an open-drain transistor is connected to the MC system reset. WDT operation is controlled by the software. The sensitivity of the ADM8324 chip to ESD is the same as for the MC.

Existing solutions for the formation of a system reset in microprocessor systems are reduced to the use of an integrated or external WDT, a system reset is performed at the input of the RST MC.

If, in the event of a failure, the MC is restarted at the RST input, then the well-known external WDTs provide functions for restoring the MK operability to the automatic or manual mode. In the stated above studies, the impact of ESDs on microcontrollers in the continuous long-term operation is not considered. Failures caused by various reasons during long-lasting operation in a complex computer system are inevitable.

Let us consider quantitative indicators of the level of structural complexity of a relatively simple, widely used microcontroller AT89S8253.

The Atmel microcontroller AT89S8253, whose release has been supported for more than 20 years, provides the following standard features: 12K bytes of in-System Programmable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, 32 general-purpose registers, 22 registers of special functions, programmable WDT, two data pointers, three 16-bit timers/counters, a six-vector, a four-level interrupt architecture, a full duplex serial port, an on-chip oscillator and a clock circuitry [11]. The AT89S8253 is a low-power, high performance CMOS 8-bit microcontroller.

As it was noted above, the failure of the MC cannot affect the operation of the external WDT, since it is not controlled by the software of the MC. Technologically, it seems possible to

introduce an independent MC software, executed as a part of the MC WDT which has autonomous power from a battery operating in the MC, into the composition of the MC. Such WDT could provide a hard restart of the MC in the absence of a signal confirming the health of the MC. However, the author of the paper is not aware of the implementation of this technical solution for WDT.

4. Materials and methods

Let us consider a possible picture of the hang (freeze) of the MC which has been exposed to ESR for a long time when the work capacity of the MC is not restored by the system reset at the RST input. Below there is presented an enlarged fragment of the program, assembler ASM51:

```
            LJMP START;      Transfer control to the program after primary microcontroller
                             reset, START mark
START:      XXX  XXXX;       MC initial settings
RESTART:    CPL  P0.0;       LED Inversion port P0.0
              XXX  XXX;      Commands of execution collection, processing and infor-
                             mation transfer
            …

              XXX XXX;       Commands of execution collection, processing and infor-
                             mation transfer
LJMP        RESTART;         completion of the program cycle, transition to RESTART la-
                             bel
              END
```

During a cyclic execution of the program (from the RESTART label to the LJMP RESTART command), information is collected from sensors and then processed, and control signals are generated. Cycle time of the process is 5 ms. At the same time, the port P0.0 forms a meander with the same period. When the MC hangs, the signal at the output of the port P0.0 is in the logical state «0» or «1».

Under the influence of ESD on the printed circuit boards (PCB) with the MC, the hang of the program was visually observed and expressed in the termination of the inversion of the glow of the control LED port P0.0. Regarding possible causes of the hang due to the impact of ESD on the microprocessor board, when replacing the above work program with a program in which the commands of collecting, processing and transmitting information are replaced with «NOP» commands, a similar hang of this program (which uses less than 1 % of registers and flash memory cells) was also observed systematically.

In the author's opinion, an avoidable failure of the MC occurs in this case either/and in synchronization and control units, instruction register, DPTR dual pointer, program counter, or program counter increment due to the influence of ESD.

This circumstance allows to make a conclusion that software methods for duplicating information in general registers or methods for preventing loops when using general purpose registers and special function registers may not give the desired result. It was assumed that the modification of the software and circuitry of the product, providing a single or multiple switching on and off of the MC without the intervention of a human operator, will ensure the restoration of the MC work capacity.

Implementation of the method consists in organizing, as a part of the MC cyclic program of the high readiness system of a number of control points, the placement of which depends on the character of the program.

At each control point, the command inverts the control signal of the selected port, for example, «CPL P0.0». As a result of the cyclic execution of the program, a control signal of the meander type of a changing structure is formed at the port output.

The duration of the logical «0» and «1» meander levels can vary in the range of 10^2 μs to 10^2 ms. If the program hangs, a constant signal with the level «0» or «1» appears at the output of the port P0.0. This signal is sent to an external WDT (Watchdog Timer External, WDE) developed in progress of the laboratory tests for AT89S8253. WDE structure and connection are shown in Fig.1 where WDI – timer input (Watchdog Timer Input), U_{SS} – voltage supply to the MC, US – timer power supply voltage, P0.0 – output of the port forming the control signal. It is important that electronic radio elements (ERE) of the WDE, such as resistor, capacitor, IRLR024 metal-oxide-semiconductor field effect transistor (MOSFET) [13], key transistors, multivibrator transistors are resistant to ESD. The effect of ESD on these elements is absent as ESD potential values do not exceed the MC destruction threshold.

WDT elements R0 and C0 form a high-pass filter (HPF). The HPF time constant is of the order of 100 ms with a capacitance C0 of about 0.1 μF and a value of R0 of about 10^6 Ohms. If the pulse repetition period corresponds to the TLO MAX (maximum time level «0» of the meander P0.0) and TL1 MAX (maximum time of level «1» of the P0.0 meander) values (see timing schemes in Fig. 2), then the pulses at the gate input G of the transistor T0 modulate the drain-source channel resistance of the transistor T0 (DS), as shown in Fig. 2 where R_H – the drain-source resistance of the closed transistor T0, R_L – the drain-source resistance of the open transistor T0.

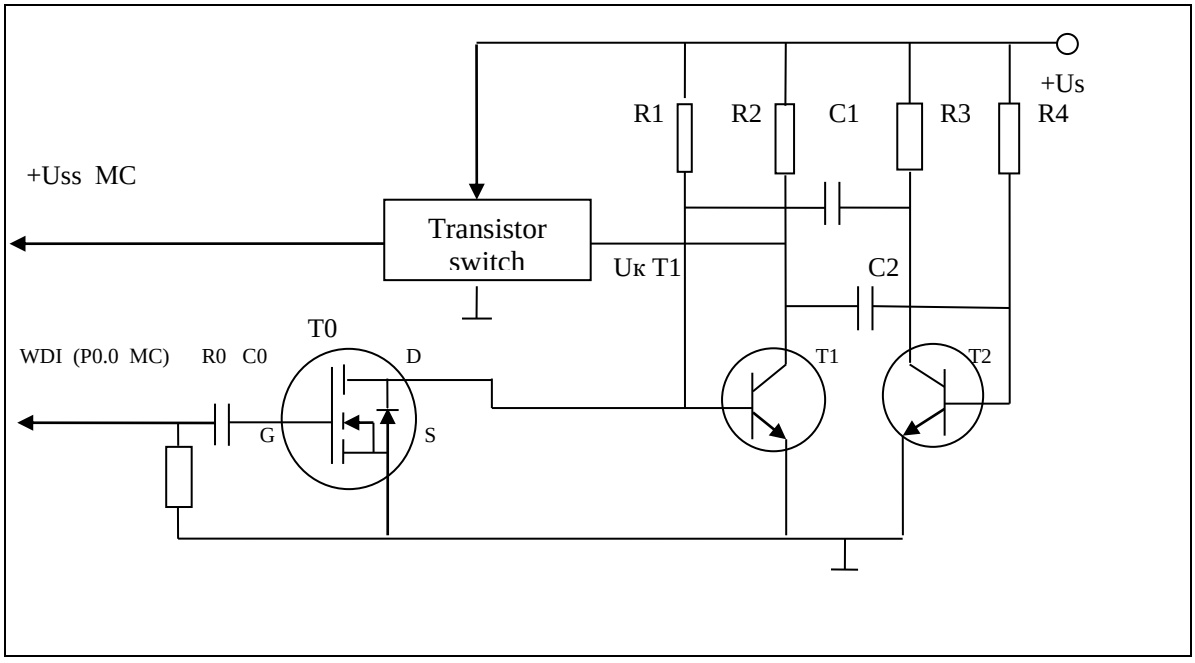

Figure 1– External Watchdog Timer (WDE)

This continuous modulation, with a time interval that does not exceed 10 ms, closes the base of the multivibrator transistor T1 (MV) on a common bus. When the capacitances C1 and C2 of the MV are about 100 μF, and the resistors R1 and R3 are about 50 kOhm, the oscillation period of MV is 5 s. The relaxation process is interrupted every 10 ms. Transistor T1 is permanently closed. The voltage Uss ≈Us is supplied to the MC through a transistor switch. The regular operating mode of MC is carried out.

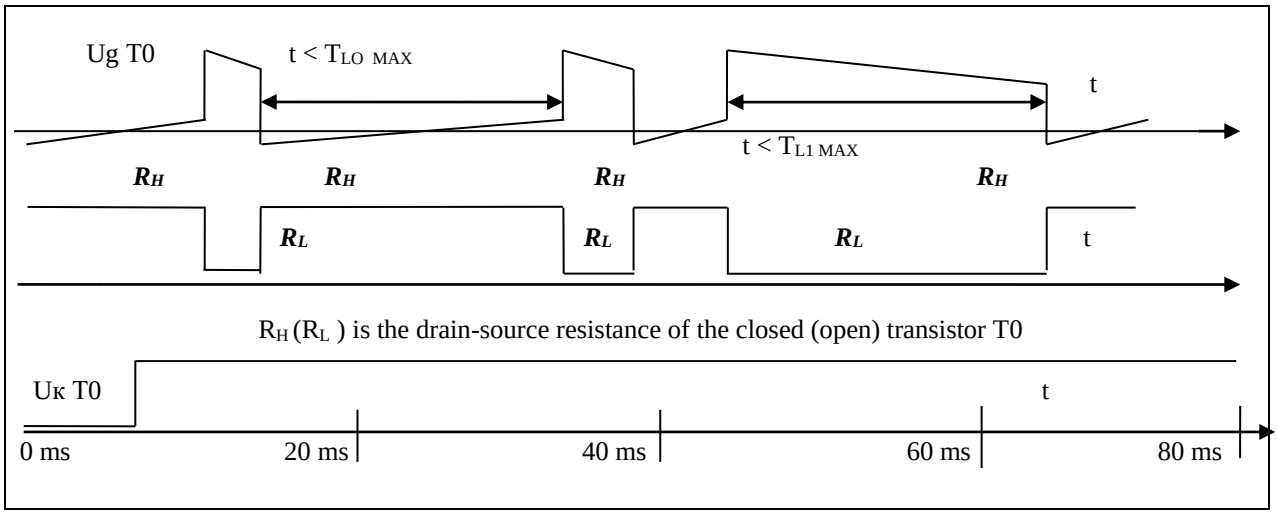

Figure 2 – Normal operation of the WDE

If there are no pulses from the P0.0 MC port and the P0.0 port hangs in the «0» state, zero voltage is formed at the HPFoutput (see Fig. 3). In Fig. 3 T_{SS} is the time of switching power supply of the MC until a successful restart, RH – the drain-source resistance of the closed transistor T0, RL – the drain-source resistance of the open transistor T0. The drain-source resistance of the closed transistor T0 is large, the MV goes into a self-oscillating mode. During one or several periods of MV oscillations, the power supply of the MC turns off and on, until the MC successfully reboots after exposure to ESD. The device goes into the regular operating MC mode. When the P0.0 MC port hangs in the «1» state, the voltage at the HPF output is also zero and the drain-source resistance of the closed transistor T0 is large.

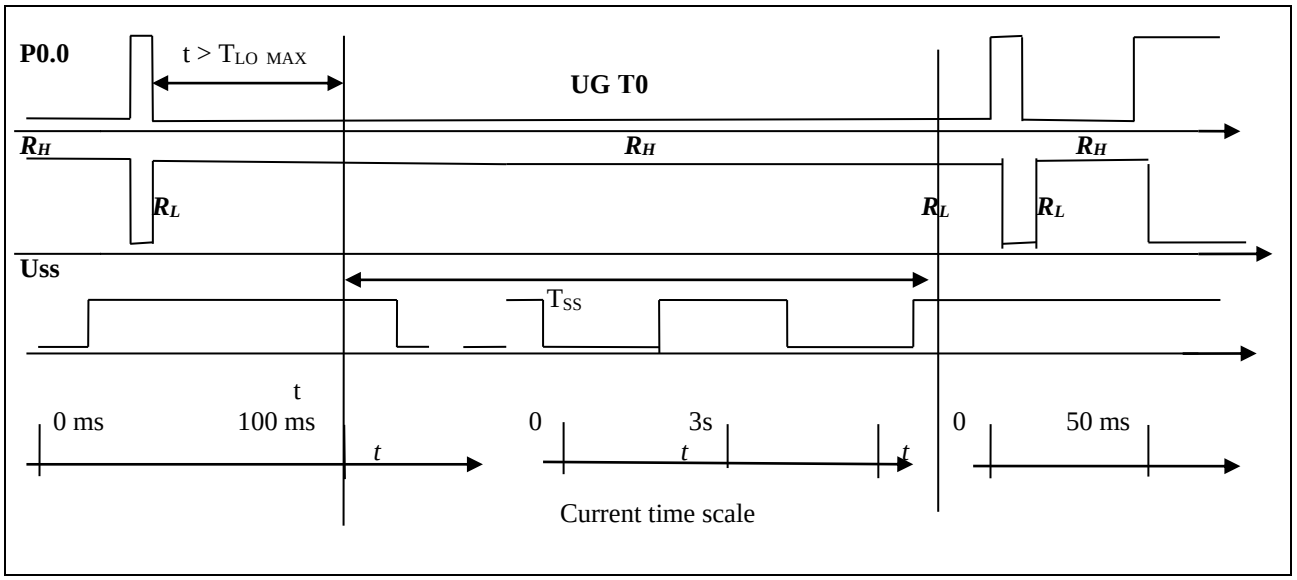

Figure 3 – Restart of the MC. The port P0.0 is stuck in the «0» state

5. Experiments

Under the influence of ESD on the AT89S8253 MC of PCB in laboratory conditions within the framework of well-known models (Human Body Model, Machine Model and Charged Device Model [14–16]), the effect of the MC hang has been observed in both contact and air discharges. Microprocessor devices were not exposed to triboelectricity and external electric field. Attempts to restart the hang of the AT89S8253 microprocessor in the mentioned above laboratory tests

were performed by applying the corresponding potential to the RST input. In most cases this operation did not restart the microprocessor.

Microprocessor systems, which are the subject of this research, have been in continuous and long-term operation in more than 500 industrial, enterprise and institutional facilities in Ukraine:

– in elevators of residential and administrative buildings in different climatic zones of Ukraine (Crimea, Donbass, cities of central regions). Grounding of electrical equipment in buildings was carried out in the ground of different conductivity or lack thereof. PCB of these elevator devices was exposed to tens of thousands of people with a wide variety of electrostatic charges and the nature of attempts to sabotage the devices. Annual springtime exacerbations of electrostatic exposures are of note as well;

– in motor vehicles. Machine bodies accumulate electric charge that does not flow to the ground;

– in security and fire alarm devices located both inside buildings and in open spaces. Sensor loops of fire and security alarm devices are particularly susceptible to atmospheric electricity [2].

Noted conditions of operation of these systems give the grounds for assuming presence of influence on them of ESR of all kinds.

The listed above objects acted in fact as a «polygon», where representative results were got, the obtaining of which laboratory tests did not provide.

Under laboratory conditions, it was decided to obtain preliminary results which could serve as a basis for making a decision on the method of removing the hang of a microprocessor device, with insignificant expenses on test equipment, in the framework of a machine model and a human body model.

If necessary, it was supposed to expose the microprocessor devices to both triboelectricity and an external electric field.

6. Results

During these tests it was found that the restart of the MC was guaranteed to be carried out by once or repeatedly turning on and off the supply voltage of the PCB chips. The hardware and software implementation of the method discussed above in the vast majority of cases provides failure associated with the impact of ESD, the restoration of the microprocessor board. So, out of 300 systems of the type [17], before the restart was introduced according to the considered method, about 10 systems hang every month. After its introduction, such failures completely disappeared.

7. Discussions

According to the author, the avoidable failures of the MC due to the impact of ESD on the MC lead to the gradual development of damage to the MC, intensifying during operation.

By the properties of the initial set of objects that are significant from the point of view of research tasks we mean the coverage of almost all possible types of ESD effects (contact, air discharges, triboelectricity and an external electric field). Then, a large number of objects across the country that used microprocessor devices (in general, about 500), where all types of ESD effects are present, allows us to consider a sample of several dozen devices representing all the options for their use investigated in laboratory conditions to be representative.

8. Conclusions

1. The scientific and technical goal achieved by this study is to increase fault tolerance of amicroprocessor device to the effects of ESD. It is beyond the scope of this paper to provide a de-

tailed theoretical justification of this method. However, the results of experimental observations obtained from more than 500 devices confirm effectiveness of this device.

2. Introduction of the proposed method increases the useful life of microprocessor systems and provides the possibility of their long-term operation in the standalone mode.

3. Operation of the system with a hard restart by turning off/on the power also showed the following particularly positive results:

– the stability of the ERE of the restart system to the effects of electrostatic electricity was confirmed;

– based on long-term observations over several years, it was concluded that restarting the system after the likely impact of ESD weakens the cumulative effect of damage accumulation.

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